

**NEWARK COLLEGE OF ENGINEERING**

**SYLLABUS AND COURSE INFORMATION**

- Course Name:** Digital Logic and Circuit Design
- Course Number:** ECET 365
- Course Structure:** 3-0-3 (lecture hr/wk – lab hr/wk – course credits)
- Course Description:** Develops the mathematics and minimization techniques together with the circuit implementation for the design of combinational and sequential digital solid-state logic circuits. Studies decoders, multiplexers, counters, registers, and PLDs. Computer and communications circuits are used as examples. Projects employ computer simulation of digital circuits.
- Prerequisites:** ECET 215 or ECE 251
- Corequisites:** None
- Required, Elective, or Selected Elective:** Required
- Required Materials:** **Text:** Name: Fundamentals of Digital Logic with VHDL Design  
Author: Stephen Brown and Zvonko Vranesic  
Year: 2008  
ISBN: 978-0-07-722143-0
- Course Outcomes:** By the end of the course students are able to:
1. Analyze and design basic combinational SOP and POS logic systems.
  2. Apply various simplification techniques to combinational logic.
  3. Apply decoders to memory systems and combinational logic
  4. Apply multiplexers to time division multiplexing systems and combinational logic.
  5. Distinguish between the various programmable logic devices and draw logic using the short hand logic commonly used in PLDs.
  6. Analyze and design basic sequential logic systems including counters.
  7. Determine waveforms and state diagrams for circuits with SR, D, JK and T type flip-flops.
  8. Design finite state machines in an efficient manner.
  9. Use the schematic capture and the VHDL language to design, simulate and troubleshoot both combinational and sequential logic using the CAD software.
  10. Present the results in a well-documented report with all logic and timing diagrams computer generated.

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**Class Topics:** Boolean Algebra                      Gates  
Combinational Logic                      Sequential Logic  
Hardware Implementations              Finite State Machines  
VHDL Design                                  Timing Analysis

**Student Outcomes:** The Course Learning Outcomes support achievement of the following Student Outcomes from the ETAC of ABET Criterion 3 requirements.

**Student Outcome 1:** An ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline.

**Related Course Learning Outcomes:** 2, 3, and 4

**Student Outcome 2:** An ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives.

**Related Course Learning Outcomes:** 6 and 8

**Academic Integrity:** Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at:

<http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf>

Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university. If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at [dos@njit.edu](mailto:dos@njit.edu)

**Modification to Course:** The Course Outline may be modified at the discretion of the instructor or in the event of extenuating circumstances. Students will be notified in class of any changes to the Course Outline.

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**Updated:** 11 March 2023