Syllabus CPT 310 Spring 2023 (Updated)

Grading:
Exam(s)
- Midterm Exam   15%
- Final Exam   20%

Homework
- Assignments   40%
- Final project   15%
- Exercises at the end of chapter

XiLinx Software: schematic editor   10%

Exams (modified for njit campus closure)

- Four versions of exams emailed to students randomly to ensure no class collaboration
- Strict 2hr time limits to return answers.
- Answers must exclude any screen shots of automated online tools, for example Karnaugh maps and state diagrams must be handwritten and scanned or pictures via phone returned.
- During exam a WebEx session will be on.

Course Summary

   The object of this course is to provide an understanding of the fundamentals of logic and computer design. The first half covers logic design; number systems, Gates, mapping (Karnaugh maps), arithmetic and sequential circuits and the second half covers digital system design; arithmetic and logic unit (ALU), sequential control design and communication between CPU and i/o devices. The course provides digital system design fundamentals while taking a gradual bottom up development of the fundamentals.

Modifications to in class lectures:

   Additional videos and PowerPoints have been added to canvas using Kaltura to cover weekly topics and exam review videos replace the final exam review.

   (students receive weekly emails about class material, and require acknowledgement to take attendance)

- ## Schedule
- Week
- 1st Course Introduction
- 2nd Binary numbers/Arithmetic Operations/BCD/Gray codes/ASCII
- 3rd Combinatorial Logic Circuits Part I / XiLinx Schematic editor Part I
- 4th Combinatorial Logic Circuits Part 2/ XiLinx Schematic editor Part2 I
- 5th Combinatorial Logic Design / Hierarch and top down design
- 6th Combinatorial Functions and Circuits
- 7th Programmable Logic arrays & devices/Decodes/Multiplexers
- 8th Midterm
- 9th Arithmetic functions & circuits
- 10th Sequential circuits
- 11th Registers and Register Transfers
- 12th Sequencing & Control
- 13th Computer Design Basics/Instruction set architectures
- 14th Input-Output and Communications
- Reading
- 15th **Final**